IN THE CLAIMS

Please cancel claims 1-16 without prejudice. Claims 17-22 are new.

The following claims are now pending in the present application:

1-16. (Cancelled)

17. (New) A semiconductor package, comprising:

a substrate that includes a top surface and an exposed external opposite surface including an inner region, an outer region, and a middle region that separates the inner and outer regions;

a plurality of contracts including a first plurality of contacts and a second plurality of contacts, said first plurality of contacts located in the outer region, and said second plurality of contacts located in the inner region, wherein the middle region is free of contacts over a distance that is larger than the smallest distances between adjacent contacts in the inner and outer regions; and

an integrated circuit that is mounted to said top surface of said substrate, wherein said first and second plurality of contacts are located respectively outside and inside a dimensional profile of said integrated circuit.

18. (New) The semiconductor package of claim 17, wherein the distances between adjacent contacts in the inner region are equal to the distances between adjacent contacts in the outer region.

19. (New) The semiconductor package of claim 17, further comprising a plurality of electrically conductive members attached to said plurality of contacts of said first and second plurality of contacts.

20. (New) The semiconductor package of claim 17, wherein said top surface of said substrate has a ground bus that is coupled to said integrated circuit and connected to said second plurality of contacts by a plurality of vias that extend through said substrate.

21. (New) The semiconductor package of claim 17, wherein said top surface of said substrate has a power bus that is coupled to said integrated circuit and connected to said second plurality of contacts by a plurality of vias that extend through said substrate.

22. (New) The semiconductor package of claim 17, further comprising an encapsulant enclosing said integrated circuit.